IN THE CLAIMS

We claim:

1. An intermediate frequency filter for use in an integrated circuit, comprising:

a first filter stage, the first filter stage including a first LC resonator; and

the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface.

2. The filter of claim 1, wherein:

the first filter stage further including a second adjustable capacitor array coupled to the LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of data storage locations, the second plurality of data storage locations programmable through the serial control interface.

3. The filter of claim 2, wherein:

the data storage locations of the second plurality of data storage locations are fuses.

4. The filter of claim 2, wherein:

the data storage locations of the second plurality of data storage locations are bits of a register.

5. The filter of claim 1, wherein:

the first capacitive array includes a first capacitor of a first magnitude coupled in series with a first switch and further coupled in series with a second

capacitor of the first magnitude, the switch controlled by a first fuse of the first plurality of fuses; and

the first capacitive array includes a third capacitor of a second magnitude coupled in series with a second switch and further coupled in series with a fourth capacitor of the second magnitude, the switch controlled by a second fuse of the first plurality of fuses, the combination of the third capacitor, second switch and fourth capacitor coupled in parallel with the combination of the first capacitor, first switch and second capacitor.

6. The filter of claim 1, further comprising:

a second filter stage coupled to the first filter stage, the second filter stage including a second LC resonator; and

the second filter stage further including a third adjustable capacitor array coupled to the second LC resonator, the third adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of fuses, the second plurality of fuses programmable through the serial control interface.

7. The filter of claim 6, further comprising:

an amplifier, the amplifier coupled to the first filter stage to receive an output of the first filter stage, the amplifier coupled to the second filter stage to provide an input to the second filter stage.

8. A circuit formed as part of a single integrated circuit, the circuit comprising:

a first amplifier;

a first oscillator;

a first mixer coupled to the first amplifier and the first oscillator;

a second oscillator;

a second mixer coupled to the second oscillator;

a second amplifier coupled to the second mixer;

a serial control module;

an intermediate frequency filter (IF filter), the IF filter including a first filter stage, the first filter stage including a first LC resonator;

the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of fuses, the first plurality of fuses programmable through the serial control module;

and wherein the second mixer is coupled to the IF filter and the IF filter is coupled to the first mixer. .

9. The circuit of claim 8, wherein the first filter stage further includes

a second adjustable capacitor array coupled to the LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of data storage locations, the first plurality of data storage locations programmable through the serial control module.

10. The circuit of claim 9, further comprising:

a second filter stage coupled to the first filter stage, the second filter stage including a second LC resonator;

the second filter stage further including a third adjustable capacitor array coupled to the second LC resonator, the third adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of fuses, the second plurality of fuses programmable through the serial control module; and

the second filter stage further including a fourth adjustable capacitor array coupled to the LC resonator, the fourth adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of data storage locations, the second plurality of data storage locations programmable through the serial control module.

11. The circuit of claim 10, further comprising:

a third amplifier, the third amplifier coupled to the first filter stage to receive an output of the first filter stage, the third amplifier coupled to the second filter stage to provide an input to the second filter stage.

12. The circuit of claim 11, further comprising:

a dual synthesizer coupled to the first oscillator and the second oscillator.

13. A method of tuning an integrated circuit, comprising:

receiving an integrated circuit having therein an intermediate filter with a first tunable capacitive array;

testing the integrated circuit;

adjusting the first tunable capacitive array responsive to the testing, to effect a change in a frequency response of the intermediate filter; and

repeating the testing and the adjusting as needed to achieve a desired frequency response of the intermediate filter.

14. The method of claim 13, further comprising:

operating the integrated circuit; and

adjusting a second tunable capacitive array to effect a change in frequency response of the intermediate filter.

15. The method of claim 14, wherein:

adjusting the second tunable capacitive array includes programming the second tunable capacitive array based on a lookup table.

16. The method of claim 15, further comprising:

constructing the lookup table responsive to the testing.

17. The method of claim 14, wherein:

adjusting the second tunable capacitive array includes internally measuring the frequency response of the intermediate filter.

18. A method of tuning an integrated circuit during operation, comprising:

operating the integrated circuit; and

adjusting a tunable capacitive array to effect a change in frequency response of an intermediate filter.

19. The method of claim 18, further comprising:

detecting a change in an operating frequency of the integrated circuit; and wherein the adjusting occurs responsive to the detecting.

20. The method of claim 18, wherein:

adjusting the tunable capacitive array includes programming the tunable capacitive array based on a lookup table.

21. The method of claim 18, wherein:

adjusting the second tunable capacitive array includes internally measuring the frequency response of the intermediate filter.

22. An apparatus, comprising:

means for filtering an intermediate frequency signal on an integrated circuit;

first means for adjusting a response of the means for filtering; and

means for programming the first means for adjusting.

23. The apparatus of claim 22, further comprising:

second means for adjusting the response of the means for filtering.

24. The apparatus of claim 23, further comprising:

means for repeatedly programming the second means for adjusting.

25. An intermediate frequency filter for use in an integrated circuit, comprising:

a first filter stage, the first filter stage including a first LC resonator of which at least a capacitor is part of the integrated circuit; and

the first filter stage further including a first adjustable capacitor array in the integrated circuit coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations.

26. The filter of claim 25, wherein:

the first plurality of programmable data storage locations are programmable through a serial control interface of the integrated circuit.

27. The filter of claim 25, wherein:

the first plurality of programmable data storage locations are programmable through a set of test points of the integrated circuit, the test points of the set of test points not directly connected to pins of the integrated circuit.

28. The filter of claim 25, wherein:

the first filter stage further includes a second adjustable capacitor array coupled to the LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of data storage locations.

29. The filter of claim 28, further comprising:

a second filter stage coupled to the first filter stage, the second filter stage includes a second LC resonator of which at least a capacitor is part of the integrated circuit; and

the second filter stage further includes a third adjustable capacitor array coupled to the second LC resonator, the third adjustable capacitor array having an effective capacitance value adjustable through use of a third plurality of fuses.

30. The filter of claim 25, further comprising:

a second filter stage coupled to the first filter stage, the second filter stage includes a second LC resonator of which at least a capacitor is part of the integrated circuit; and

the second filter stage further includes a second adjustable capacitor array coupled to the second LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of fuses.

31. The filter of claim 30, wherein:

an inductor of the second LC resonator is separate from the integrated circuit.

32. The filter of claim 30, wherein:

an inductor of the second LC resonator is integrated into the integrated circuit.

33. The filter of claim 25, wherein:

an inductor of the first LC resonator is separate from the integrated circuit.

34. The filter of claim 25, further comprising:

an inductor of the first LC resonator is integrated into the integrated circuit.

35. An intermediate frequency filter for use in an integrated circuit, comprising:

a first filter stage, the first filter stage including a first LC resonator;

the first filter stage further including a first adjustable capacitor array coupled to the first LC resonator, the first adjustable capacitor array having an effective capacitance value adjustable through use of a first plurality of programmable data storage locations, the first plurality of programmable data storage locations programmable through a serial control interface;

a second filter stage coupled to the first filter stage, the second filter stage including a second LC resonator;

the second filter stage further including a second adjustable capacitor array coupled to the second LC resonator, the second adjustable capacitor array having an effective capacitance value adjustable through use of a second plurality of fuses, the second plurality of fuses programmable through the serial control interface.

a third filter stage coupled to the second filter stage, the third filter stage including a third LC resonator;

the third filter stage further including a third adjustable capacitor array coupled to the second LC resonator, the third adjustable capacitor array having an effective capacitance value adjustable through use of a third plurality of fuses, the third plurality of fuses programmable through the serial control interface.

36. The filter of claim 35, further comprising:

an amplifier, the amplifier coupled to the third filter stage to receive an output of the third filter stage, the amplifier having an output;

a fourth filter stage, the fourth filter stage including a fourth LC resonator, the fourth filter stage coupled to the output of the amplifier;

the fourth filter stage further including a fourth adjustable capacitor array coupled to the first LC resonator, the fourth adjustable capacitor array having an effective capacitance value adjustable through use of a fourth plurality of programmable data storage locations, the fourth plurality of programmable data storage locations programmable through a serial control interface;

a fifth filter stage coupled to the fourth filter stage, the fifth filter stage including a fifth LC resonator;

the fifth filter stage further including a fifth adjustable capacitor array coupled to the fifth LC resonator, the fifth adjustable capacitor array having an effective capacitance value adjustable through use of a fifth plurality of fuses, the fifth plurality of fuses programmable through the serial control interface.

a sixth filter stage coupled to the fifth filter stage, the sixth filter stage including a sixth LC resonator; and

the sixth filter stage further including a sixth adjustable capacitor array coupled to the sixth LC resonator, the sixth adjustable capacitor array having an effective capacitance value adjustable through use of a sixth plurality of fuses, the sixth plurality of fuses programmable through the serial control interface.